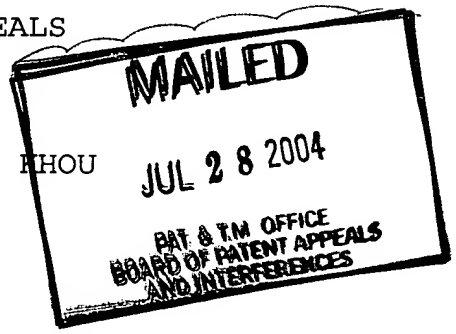
The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES



Ex parte JACQUES WONG, BENG CHEW KHOU
and BOON PIAW TAN

Appeal No. 2003-1202
Application 09/517,518

ON BRIEF

Before HAIRSTON, GROSS and NAPPI, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 3 and 5 through 17. In an Amendment After Final (paper number 12), claim 10 was amended.

The disclosed invention relates to a method of synthesizing a register transfer level (RTL) based design by synthesizing sub-

modules of a top-level design. According to appellants (specification, page 1), the synthesis of RTL based design is a process of translating a hardware descriptive language (HDL) coded design to required technology logic gates based on library technology and timing constraints.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A method of synthesizing a register transfer (RTL) based design of a system comprising the steps of:

determining a plurality of sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing gate-level designs of the sub-modules based on the determined time budgets for the individual sub-modules;

testing the gate-level designs for conformance with gate-level design requirements of the individual sub-modules, then integrating the gate-level designs of the individual sub-modules to form a top level design;

testing the top-level design for conformance with top-level design requirements; and

generating a top-level netlist when the top-level design conforms to the top-level design requirements.

The reference relied on by the examiner is:

Dupenloup	6,295,636	Sept. 25, 2001 (filed Feb. 20, 1998)

Claims 1 through 3 and 5 through 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Dupenloup.

Reference is made to the briefs (paper numbers 15 and 17) and the answer (paper number 16) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the anticipation rejection as to claim 1, and reverse the anticipation rejection as to claims 2, 3 and 5 through 17.

Turning first to claim 1, appellants argue (brief, pages 4 through 7) that Dupenloup does not teach any form of testing of gate-level designs of individual sub-modules. The examiner contends (answer, pages 3, 4 and 6 through 8) that Dupenloup teaches verification/testing of gate-level designs of individual sub-modules via the iterative loop 455 (Figure 19; column 43, lines 8 through 32).

We agree with the examiner's conclusion (answer, pages 7 and 8) that:

> The Dupenloup passage at column 43 further discusses the characterization of *each* module. Column 43, lines 16-18 states:

> Top-down characterization provides constraints, time budgets, and other information required to be met by ***each*** of the modules. (emphasis added).

Here, Dupenloup's use of the word "each" signifies that Dupenloup applies to IC design sub-modules and modules. "[E]ach of the modules" broadly references modules and/or submodules.

Dupenloup discloses the existence of a testing or verification process wherein top-down characterization and bottom-up resynthesis are conducted until all constraints are met and the gate count is stable. Column 43, lines 21-25 states:

> The top-down characterization step and bottom-up resynthesis steps are iterated until all constraints are met by each of the modules being synthesized and gate count for each of the modules are stable.

Here, Dupenloup provides evidence of the existence of a gate level implementation coupled with subsequent testing through iteration of the top-down characterization and bottom-up resynthesis.

Appellants assert that "nowhere in Dupenloup does the term 'test' occur in conjunction with individual sub-modules." (Appellants' Argument, page 6). While this may be true of Dupenloup, the same also applies to Appellants' specification. Nowhere in Appellants' specification do Appellants use the term 'test' in conjunction with individual sub-modules. Appellants, like Dupenloup, reference a [sic, an] iterative process, inherent to any testing procedure, of optimization and re-synthesis until specified requirements are satisfied. Appellants' own Figure 3 . . . illustrates the procedure.

In view of the examiner's analysis, the anticipation rejection of claim 1 is sustained.

Turning next to claims 2, 3, and 10 through 17, the examiner is of the opinion (answer, pages 9 and 10) that Figures 1 and 19 of Dupenloup show the generation of gate-level netlists for sub-modules. We disagree with the examiner's assessment of the teachings of Dupenloup. Although Figure 1 of Dupenloup shows the generation of a gate-level netlist, it is not done at the sub-module level as required by the noted claims. Figure 19 of Dupenloup is concerned with sub-modules, but the final netlist 456 is not for each of the sub-modules as required by the noted claims. Thus, the anticipation rejection of claims 2, 3, and 10 through 17 is reversed.

Turning lastly to claims 5 through 9, we disagree with the examiner's finding (answer, pages 11 and 12) that Dupenloup teaches (column 12, lines 43 through 48) static timing analysis of the individual sub-modules. As correctly argued by appellants (reply brief, page 8), Dupenloup is completely silent as to such a teaching. Accordingly, the anticipation rejection of claims 5 through 9 is reversed.

DECISION

The decision of the examiner rejecting claims 1 through 3 and 5 through 17 under 35 U.S.C. § 102(e) is affirmed as to claim 1, and is reversed as to claims 2, 3, and 5 through 17.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON)
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